1.2 ICs for Mobile Multimedia Communications

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I. INTRODUCTION

The seemingly endless advancement of silicon technology has enabled the emergence of mobile broadband communication systems for voice, data and video transmission with good connectivity and proper quality of service. Devices are being fabricated using processes managed at atomic levels while IC design involves detailed systems engineering, including the incorporation of application content. Data-rate and mobility trade-offs and different standards like 2G, 3G, Bluetooth, WLAN, GPS and digital video broadcasting are leading to multimode requirements and issues relating to coexistence and inter-working of these different technologies must be solved. Furthermore, secure data transfer and encryption are vital for the networked world.

Together, these issues lead to challenging architectural requirements such as re-configurability and programmability because of the growing importance of multimode and multi-standard solutions. While parameters like data-rate and algorithmic and circuit complexity have changed approximately exponentially with time, there has not been much improvement in the battery capacity. For this reason, a key consideration for mobile products is energy management and power reduction.

In this context the introduction of platform concepts including analog and RF at the most practical cost, power-levels and form-factors are key requirements for system-on-chip and system-in-package solutions for current and future mobile multimedia terminals.

This talk will explore current multi-million transistor IC's with multi billion operations per second of signal processing and analog and RF capabilities for mobile multimedia communications. It will consider special requirements on wafer processes like leakage and analog and RF capabilities and will look at how R&D engineers bridge the world of system-level design, silicon and software and, of course, new challenges for the future will be considered and explored.

II. EMERGING BROADBAND WIRELESS TECHNOLOGIES

At the current growth rate, the number of worldwide subscribers of cellular services is expected to exceed 1.5 billion by 2007. Today, cellular services for voice communications are primarily based on 2G systems, such as GSM and CDMA. However, with the rising demand for data services, the emerging 2.5G and 3G systems such as EDGE/GPRS and UMTS/CDMA2000, are playing an increasingly important role. Further, other technologies like Bluetooth, WLAN, UWB, A-GPS and DVB-H are enabling multimedia services for feature-rich handsets. Figure 1.2.1 shows that the mobile device is turning into an "All-in-One Solution" [1], [2]. In addition to all the radios and base-band signal processors, the battery and power management unit must support additional power-hungry features such as color LCD and 5Mpix camera. To achieve acceptable power consumption, talk time, form factor and performance the latest CMOS technologies with their increased integration capabilities must be used.

The huge volume of 780 million produced mobile handsets in 2005, the CAGR of 7.5% (Source: Gartner Dataquest, July 2005) and an exponential increase in circuit complexity per phone makes this industry a main contributor financing the process roadmap and production facilities.

From Fig. 1.2.2 we can see the exponential cost curves for process platform and production facilities. At the same time the average handset selling price is stagnating.

Cellular

GSM is the most-popular worldwide cellular standard in use today, with over 75% of the total cellular market. GSM CMOS transceivers on the market today are based on multi-chip solutions. RF transceivers are based on specialized RF technology, which does not lend itself well to high levels of integration at low cost. However, single-chip CMOS solutions have been announced recently.

In Fig. 1.2.3 a fully-integrated quad-band GSM and GPRS phone in 130nm CMOS achieving excellent performance parameters such as receiver sensitivity and power dissipation is shown.

The demand for higher data rates in a cellular environment drives the progress in UMTS mobile systems with its flavors WCDMA, CDMA2000, TD-SCDMA. While the deployment of the equipment for Release-99/Release-4 of WCDMA is far from complete, the first field tests for data-rates of up to 3,6MBit/s (HSDPA) already started and integrated circuits for data-rates of up to 7,2MBit/s are under development. A further step to increase data rates will be the use of several receive and transmit antennas. Today the base stations already use this feature. On the terminal side, the available spatial separation will constrain whether a modem with more than two antennas will be beneficial in a notebook or a mobile phone. On the system side, a change of the wireless standard is mandatory. A rather quick and straightforward but still effective way is to simply use two receive antennas at the terminal without any changes of the transmission standard. Such devices will hit the market within the next two years.

WLAN and UWB Support in Addition to Bluetooth and Infrared (IR)

Dual mode phones that integrate not only cellular but also WLAN as network access technologies have already been introduced to the market. These phones also include Bluetooth and infrared wireless peripherals; and soon UWB will be a new addition to broadband wireless technologies.

Mass-consumer-market wireless applications set strict requirements on cost, dynamic range, power consumption, and the number of external components used in the system. These constraints have already been applied to Bluetooth chips and are now being applied to WLAN SoCs. Correspondingly, many of the most integrated solutions are implemented in deep-submicron CMOS technologies which allow the full integration of the MAC and the PHY layers on the same die. These highly integrated low-cost low-power ICs open the door for the application of WLAN in mobile terminals. Further, they are applicable in many other embedded and non-embedded applications. WLAN-enabled printers, cable modems, set-top-boxes, digital cameras, and game consoles, are just a few further examples of integration of WiFi in various types of consumer electronics. The high-level of integration of such a system-on-chip changes the economics of WiFi solutions, and enables the continued price reduction of WiFi-enabled consumer electronics.

Ultra-wideband technology is a new member in the family of broadband technologies. In the public discussion it is one of the hot topics in the wireless connectivity arena today, although UWB has been around since many years, originally invented for military applications. The current hype surrounding UWB shows that there is still space for new concepts with even higher data-rates for short-range wireless connectivity.

Key parameters for such UWB systems are data-rates of up to 500 Mbps over distances up to 10 meters, at comparably low transmit power levels (around -8dBm at the antenna).

Besides regulatory issues, a widely accepted standardization is a prerequisite for a successful market introduction. Although there is still [Nov.'05] the deadlock in the IEEE 802.15.3a task group [3], [4], other alliances like Wireless-USB [4] and WiMedia [5] will pave the way for global acceptance of UWB technology, in PC-oriented as well as mobile devices.

To the delight of today's engineering community UWB chip design tends to be a challenging task. Due to the wideband and pulse-based nature of UWB signals, a lot of concepts and circuit techniques that are well known and understood from narrowband systems cannot be applied any longer. To give an example, the frequency synthesis for multi-band-OFDM UWB systems requires three different LO frequencies of 3,432GHz, 3,960GHz and 4,488GHz for band-group 1. A crucial requirement is fast hopping between those frequencies, with a hop-time of <9,5ns for the whole receiver. This prevents the use of a single PLL with programming reference or feedback clock to switch between channels, due to the slow closed-loop response, typically in the order of micro seconds. The easiest solution is to take one dedicated PLL for each required LO, but at the cost of larger area and power, especially when higher band-groups shall be supported as well. An alternate approach is to use a single PLL combined with mixers to achieve the fast hopping requirement [3]. A major challenge for all UWB synthesis approaches is to reduce all unwanted spurious components to an acceptable limit, and to achieve the integrated phase noise requirements of around 2deg RMS. Especially at the higher band-groups this is on the edge of the capabilities of currently published frequency synthesizers.

Global Positioning System (GPS), FM Radio and Digital TV

Global positioning systems and tuners for FM radio and digital TV will also become integral part of future handsets.

Cellular telephones with embedded GPS function will be a reality in the near future. Services such as driving directions, position-based services such as identifying closest banks or restaurants, and tracking of people for safety or in emergency situations are already being deployed by wireless network operators. In mobile phones, assisted GPS (A-GPS) is used to improve the performance by using an assistance server and a reference network for range measurements and position solutions. The assistance server communicates with the GPS receiver via a wireless link.

A major challenge for the A-GPS chip, consisting of RF-front-end and base-band processor, is to achieve a power consumption of significantly less than 50mW during continuous A-GPS navigation. Required RF performance is to achieve a receive sensitivity down to -160dBm, NF better than 5dB, gain of more than 35dB and 1dB compression point of better than -30dBm [7].

FM stereo radio receivers for mobile terminals require low power consumption with digital tuning, fully integrated IF filtering and demodulation. Major design challenges are: optimum noise figure (sensitivity), accurate tuning (match to VCO), reliable control at high Q's and optimum large signal behaviour.

Finally, digital TV is also moving into the handset. It is expected that the acceptance of mobile TV will be very high, with mobility and flexibility being the strongest perceived benefits. The content in highest demand is expected to be news and regional information.

Major design challenges for the digital TV tuner are power consumption, fitting large memories in the order of 5Mbit on chip, and achieving the required performance in the cellular environment (C/N, Doppler, Impulse interference). One of the future standards for digital video broadcast will be DVB-H (Digital Video Broadcast – Handheld) with field-trials in several European cities already ongoing. Major performance targets for DVB-H are: Power consumption of less than 50mW, data rate of up to 15Mbit/s, operation in a large single frequency network, reception at high driving speeds, only one antenna and handovers with single front-end. Figure 1.2.4 shows the power consumption of DVB-T tuners over the years, and compares it with the requirement for DVB-H [6]. Based on the introduced time-slicing technique, the demanding <50mW target is achievable.

III. SECURITY IS ALWAYS AN ONGOING RACE — TAKING THE UNCERTAINTY OUT OF COMMUNICATION

One of the main tasks of a Subscriber Identification Modules SIM is to authenticate a user against the mobile phone network. The cryptographic algorithms that are used here are present as "mirror" parts in both mobile handset and base-station. Therefore they have to be located in the SIM chip software or hardware.

Smartcard- and security ICs are embedded cryptographic security processors and have to face special challenges concerning architecture, design methodology and technology [8]. The requirements for power consumption and performance are quite contradictory. On one hand, embedded Java capability requires a powerful CPU core, but on the other hand the contactless mode of operation requires lowest power consumption of just a few mW.

As shown in Fig. 1.2.5, smartcard ICs have specific coprocessors for efficient execution of several cryptographic algorithms, and a set of peripherals to enable a flexible use of the controller for many kinds of applications. The most important requirement of security ICs is their resistance against attacks.

To achieve intellectual property protection for the card manufacturer and the providers, amongst others, state-of-the art products are equipped with encrypted memory (MED, memory encryption/decryption device). This feature allows the operating system to be completely encrypted in the ROM and the EEPROM data, so that an attacker, reading out the memory areas, would only gain useless information. Also, high-security cards do not use standard CPU cores, but proprietary high-security cores containing integral security concepts. This allows the secret and valuable content of a SIM card, including operating system, firmware, application software, algorithms and last but not least the secret keys, to be protected in a very efficient way. An active shield is another, very effective protection against many kinds of physical attacks, not only against memory manipulation. Until today, numerous countermeasures have been developed and tested with simulated and real attacks. By nature, the research does not stagnate in this particular field. The development of new technologies for attacks spurs on the conception and realization of new counter-measures and the evaluation of methods for testing of security functions. Proactive thinking allows us to predict future attack mechanisms and to integrate security features against such threats today.

IV. ARCHITECTURAL AND DESIGN CHALLENGES

The performance and complexity trends in ICs for mobile multimedia communications are generating many design challenges. These devices incorporate a significant amount of algorithmic complexity encompassing entire transceiver systems and application engines.

Many of the chips incorporate fairly sophisticated RF- and analog modules. The RF and A/D and D/A converters are generally pushing the state-of-the-art in speed and precision, coupled with the fact that they must be implemented on the same substrate as millions of transistors of digital circuitry switching at high speeds.

Furthermore, for cost reasons, a pure digital CMOS process is preferred, which eliminates any analog options such as double poly. It is also essential that the RF and analog designers use robust architectures and circuit design techniques that are highly insensitive to process and temperature variations. Ideally, the yield of the overall chip should be determined primarily by the defect density. Another issue that is continually faced in mixed-mode design is the difficulty in scaling to smaller process geometries, especially due to the corresponding reduction in supply voltages. There is always a compelling reason to scale the digital circuitry to take advantage of the lower supply voltage to reduce power dissipation. However, the reduced power supply voltage significantly increases the design challenges for the RF and analog circuitry. The availability of dual-oxide processes can partially offset this problem by allowing a higher-voltage RF and analog section and a lower voltage digital section on the same chip. This does help mitigate the situation, but inevitably, there will be a compelling demand to operate the RF and analog sections at voltages lower than 1V.

The RF Transceiver

Unlike SiGe or bipolar implementations, it is proven that RF transceivers can be integrated successfully in standard CMOS. A major difficulty is that MOS transistors exhibit much higher flicker noise than bipolar transistors. Flicker noise is the main obstacle for mixers needed to convert RF-signals directly into base-band signals in a direct-conversion receiver. A low-flicker-noise direct-conversion CMOS mixer enabling a receive sensitivity of better than -113dBm for GSM is a significant step towards low-cost, miniaturized radio receivers.

High performance RF in standard CMOS enables the integration of the RF-transceiver and the digital base-band processor on the same chip, leading to lower costs, less space, and even to some extent reduced power consumption.

Looking at further advantages like savings in process development and streamlined production, it is evident that RF CMOS will dominate the further evolution of RF transceivers and system on chip integration. Further challenges for efficient RF transceiver implementations are the multi-carrier and OFDM based technologies with their high peak to average power ratios.

The next step is to further develop the architectures towards efficient multi-mode capability as shown in Fig. 1.2.6. It is a challenging job to find the right tradeoffs between cost, configurability, performance, and power consumption [9]. By re-using the receiver and/or transmitter for several different standards with different bandwidths, significant savings in circuit complexity and silicon area can be achieved. However, having the performance targets set by single-system solutions, which are highly optimized for low power consumption, causes some headache to the system designers. The problem becomes even more challenging when the issue of the multi-mode antenna front-end is added. Switching the antenna port to something like seven different receiver inputs and five different PA outputs with all the accompanying filters and duplexers is not only a complex technical problem on its own, but is also strongly coupled to the choice of the transceiver architecture. Most likely the wireless future will ask for a well-balanced combination of the optimum RF / front-end architectures and module technology as shown in Fig. 1.2.7.

Analog Circuit Concepts

With each generational advance in lithography the thickness of the gate-oxide and power-supply voltages are reduced. This presents a particular challenge to the analog-circuit designer, who is constantly battling to preserve a sensitive signal above the "noise floor".

In some cases, the analog circuitry can be moved to a separate chip with higher supply voltages, implemented in older technology. In other cases, however, the arguments for a single chip including digital, analog and RF are compelling, mostly for cost reasons. This is leading to analog- and RF- circuits that can operate on supply voltages of 1V or even below. Furthermore, these circuits must cope with other special challenges posed by fabrication processes at 90nm and below like high leakage currents and low gain, for example.

Advances in signal processing are mainly measured by increasing speed (or bandwidth) and increasing dynamic range (or resolution). Digital-to-Analog Converters (DACs) are a key element in the signal chain, taking the signal from the digital domain back to the "real world" of analog signals. In many cases, the DAC can be the ultimate performance-limiting link in the signal-processing chain.

In the digital world key challenges are low silicon area and low power dissipation. The major lever to achieve this is the further development in process integration, i.e. the ITRS roadmap going down to finer and finer feature pitches. In digital circuits we are somewhat worried about side effects like increased leakage, but in analog the situation looks much worse. Analog designers do not like small devices. The main challenges are to use the base process without an enhanced feature set, to live with the same supply voltage as the digital core devices and to track down the power dissipation to its minimum. At the same time we face the request for new services with increased bandwidths, several of them running in parallel. Figure 1.2.8 shows some popular communication standards with respect to their requirements on A/D-conversion. We see the effective resolution versus the required analog bandwidth. We can see two trends: The points are roughly aligned along a constant resolution-bandwidth product (corresponding to the same "difficulty-to-achieve") and the trend goes from upper–left to lower-right. This is well aligned with our process development which also goes towards lower voltages and higher speeds.

It may not be necessary for every one of the services mentioned previously to coexist within the same system, but the trend for universal networking devices is clearly seen. One way to achieve an enhanced feature set within reasonable time-to-market is the system-in-package (SiP) approach. In fact quite a lot of effort is put into the development of new packaging technologies to enable a further dimension of system integration in a cost-friendly and space-saving manner. However, it seems that for mass production SoC integration is still preferred, requiring clever solutions to the problems this poses.

For analog design, this means that we have to implement a lot of different feature requests with low area, low power and in a digital-compatible way. The guiding principle must be a clever system partitioning with the highest possible re-use of analog building blocks we can achieve. In the past we have seen some approaches to build re-configurable analog. The classic approach is to exploit the inherent speed (over-sampling) – resolution tradeoff in a sigma-delta converter. Quite a lot of modern cellular receivers digitize their data with such a programmable device. This is accompanied by band-switchable frequency synthesizers. Based on the fact that most SC-circuits use pretty much the same components, we have seen a pipeline – sigma-delta hybrid. At the last ISSCC devices were shown with demand-oriented power dissipation and in ISSCC 2004 we saw a converter array which is inherently reconfigurable by selecting the number of active converters.

Of course all these efforts have to go into our digital mainstream process technologies. In ISSCC 2004 the first 90nm analog designs have been presented, with even more of this kind in 2005. We are ready to see the first presentations of 65nm designs. On this ISSCC we will even see the first attempts of building analog circuitry in FinFET-technology. Figure 1.2.9 shows a recently realized fully operational Miller amplifier using FinFETs [10].

A powerful digital technology can of course also be exploited in order to enhance our analog capabilities. Self-calibration of A/D converters was already demonstrated in the 80's. Nowadays, the methods have become more sophisticated and numerous approaches have been demonstrated especially in the field of pipelined converters. However, benefits of digital control and signal processing are not limited to A/D-converters; we also can use it for other purposes like I/Q-mismatch estimation and calibration. Furthermore, digitally-assisted pre-distortion in power amplifiers (PA) in order to raise their efficiency is a field of active research.

Base-Band Signal and Data Processing Challenges

The "best" architecture for efficient base-band processing is very dependent on the application. There is a clear difference between the highly regular data streams ('data flow') occurring in signal processing, and the irregular data streams ('control flow') occurring in control processing. Undoubtedly, debates on which architecture is superior will continue: CISC vs. RISC, DSP vs. NSP or superscalar vs. VLIW parallel processing. For battery operated mobile devices it is certainly most important to achieve an efficient implementation in power and area. In practice it is proven that fully programmable architectures can have differences in their efficiencies that can differ even by orders of magnitudes. Therefore, achieving low-power and small chip area combined with flexibility in terms of programmability requires a clever hardware/software split and chip architecture. Further, for a low-power design, all parameters of the power equation must be tackled simultaneously (Fig. 1.2.10).

Figure 1.2.11 shows the silicon system platform for a mobile device. The chip consists of a modem subsystem optimized for the implementation of modulation and coding algorithms and the application subsystem for multimedia processing like 3D graphics and security.

In the modem subsystem, major functional challenges like channel estimation, interference compensation, equalization, redundant coding and Viterbi / turbo decoding have to be performed under the constraint of very limited computing time. This requires an efficient architecture and scheduling.

In the application subsystem very complex functional modules are the video, 3D-graphics and security processing.

To achieve an efficient implementation, in both the modem subsystem and application subsystem, hardware accelerators are required for the processing of these computation-power intensive tasks.
The system backbone consists of the bus system, connecting the functional blocks and the controller for the external memories. The dataflow between the different functional blocks and on- and off-chip memories must be analyzed in detail in order to enable the required performance level without excessive power consumption and area overhead.

Memories

For the memories used in wireless applications, the continuing trend towards higher density, higher bandwidth, less power consumption and smaller packages will continue to drive memory technology, architecture, design and packaging to new levels.

While today's feature phones are equipped with about 64MB volatile (DRAM) memory and 64MB non-volatile (Flash) memory, enhanced entertainment and gaming applications will require substantially increased memory densities for storing all the new applications as well as user data like MP3 files or MPEG encoded videos.

These applications require not only fast data processing, but also fast memory access. For the DRAM, this is accomplished by the transition to low-power double-data-rate (LPDDR) architecture, wider data busses (×32), and clock frequencies ranging from today's 133MHz to 200MHz and beyond in 2007.

Reducing the power consumption, both in active and idle states, remains the biggest challenge. Today's wireless memories operate from a 1.8V supply, and with advanced process technologies a transition to 1.2V is expected to occur in 2008 / 2009. Leakage currents of advanced CMOS memory technologies are the biggest threat for battery standby time. For wireless memories, the technology platforms used by commodity DRAM need to be enhanced by special low-leakage elements, and sophisticated circuit design measures help to further reduce the effect of leakages. Integrated temperature sensors adjust the refresh rate to the minimum required for reliable data retention.

Finally, on the packaging side, the space restrictions in wireless products have led to 3D assembly in form of memory stacking as multi-chip packages (MCP) or package stacking as so-called package-on-package (POP). In all cases, silicon dies will be thinned down to 50 to 100µm. While this die stacking reduces the parasitics in the interconnect and thus allows higher data rates, the direct thermal coupling of various dies in a single package creates new challenges for thermal management.

Power Management in Mobile Terminals

Functionality upgrades, while retaining high system efficiencies and maximized battery life, high levels of integration and minimized board space have driven the development of advanced and highly integrated solutions for power supply generation and battery management.

Complex systems require a smart partitioning of power management functions including the capability to deal with a wide battery voltage range. Intelligent power management systems consist of efficient power generation like programmable switch-mode regulators for low voltage applications. Digital control enables dynamic management of power conversion (wake-up, sleep, interrupt-functions, voltage scaling).

Power Management ICs are application-specific integrated circuits (ASICs), which need to combine these customer demands at reasonable costs in small packages. Power management units need both analog and digital functionality and are based on standard CMOS technologies. Optimized CMOS technology options (thick metal stack, thick oxide device) allow handling of the higher internal currents (~1A) and higher system voltages (battery ~5.5V, charger ~15V).

The current generation of a power management unit (Fig. 1.2.12) for mobile phones provides the following components, and even these will need to increase for future applications:

- A range of low dropout regulators (16) depending on the number of functions [11]
- Buck converters to control low voltage system circuits (2)
- A boost converter to enable white LED supply
- Battery charging and battery management circuits
- LED drivers with PWM outputs (4)
- A USB transceiver and an I2C interface

• A audio power amplifier
• A reset management and digital control circuit
A small package (121 pins including thermal ground pins) minimizes board space but demands thermal management to keep the heat dissipation issue under control .

V. SUMMARY AND CONCLUSIONS

Low-power wireless technologies and advanced integration continue to open up new opportunities in a variety of applications. The main challenges are the further reduction of the power and the continued system miniaturization. Innovative new concepts such as low-power SoCs, on-chip antenna integration and more efficient power-management and power-amplifiers are key requirements.

Additional challenges in the nanoscale-era include design for manufacturability of such miniaturized systems while maintaining signal integrity. As we enter the era of mobile multimedia more electronic systems will be integrated on mechanically flexible substrates such as plastics and therefore new integration technologies need to be developed.

The development of high-performance, low-voltage circuits will be one of the most significant R&D challenges facing the RF and analog IC design community.

In conclusion, broadband mobile multimedia chip design includes very interesting challenges and perspectives for IC architects and design engineers. These design challenges are difficult enough to master for any given process technology, but when one considers how rapidly new generations of process technology become available, the scope of the design challenges becomes enormously complex. Process engineers appear to be on a solid roadmap to enable the one billion transistor chip in the near future. However, design engineers may have a difficult time to find out how to use all those transistors and gates, particularly while maintaining acceptable power consumption. IC design will continue to be full of challenge and excitement for professionals in this area, but requires dedication and hard work.

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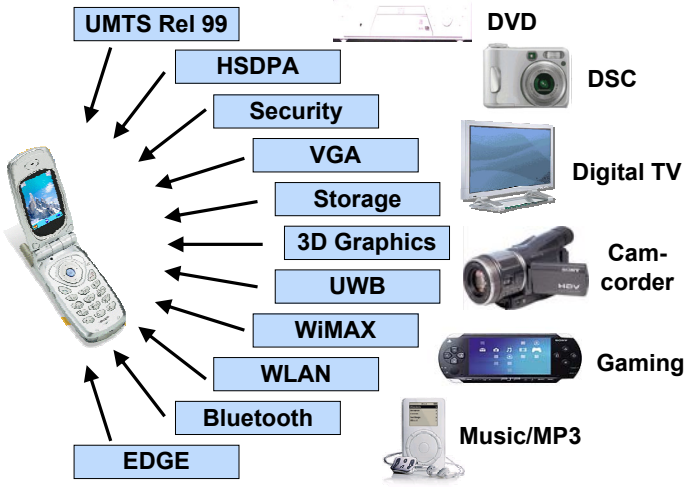

Figure 1.2.1: Mobile devices are turning into "All-in-One" solutions.

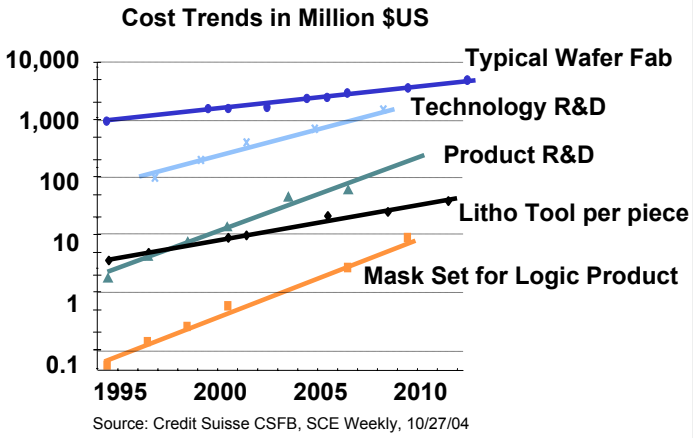

Figure 1.2.2: Semiconductor technology cost trends.

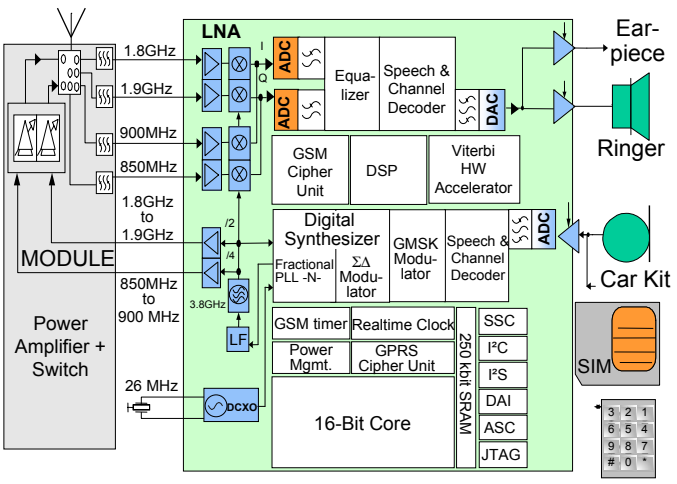

Figure 1.2.3: Single-chip, quad-band GSM/GPRS-phone.

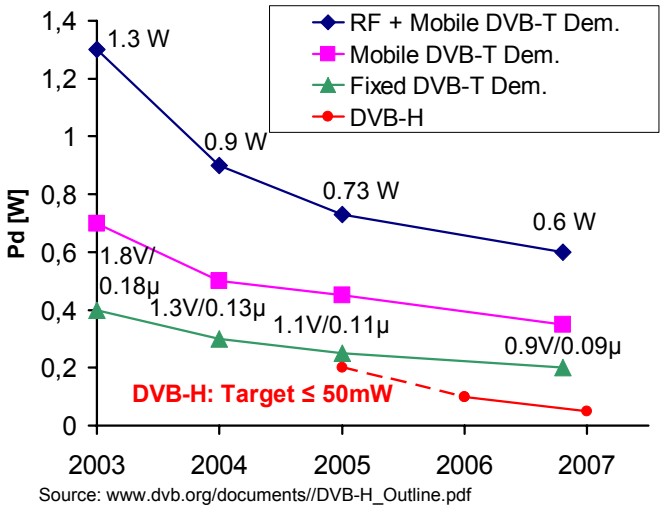

Figure 1.2.4: Power consumption of digital-TV receivers.

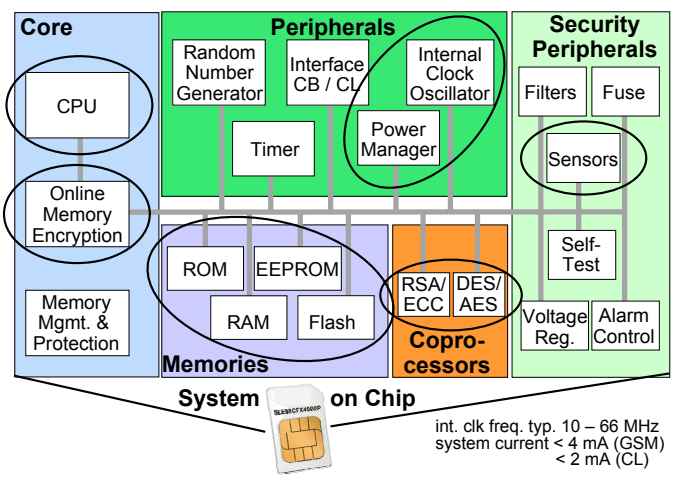

Figure 1.2.5: Smart card block diagram.

No or small resource sharing between different modes to achieve low power consumption and high performance.

Key challenge for system architecture and circuit design:

Reuse circuit blocks for different modes while maintaining performance and power consumption.

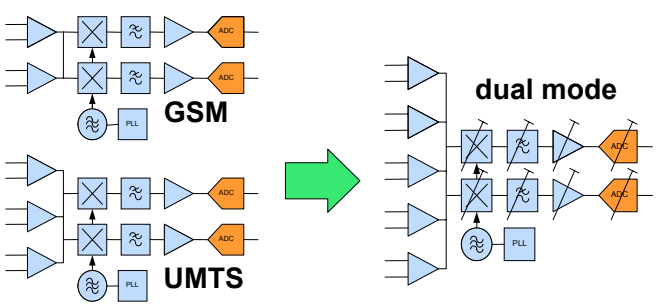

Figure 1.2.6: The transceiver "multi-mode challenge".

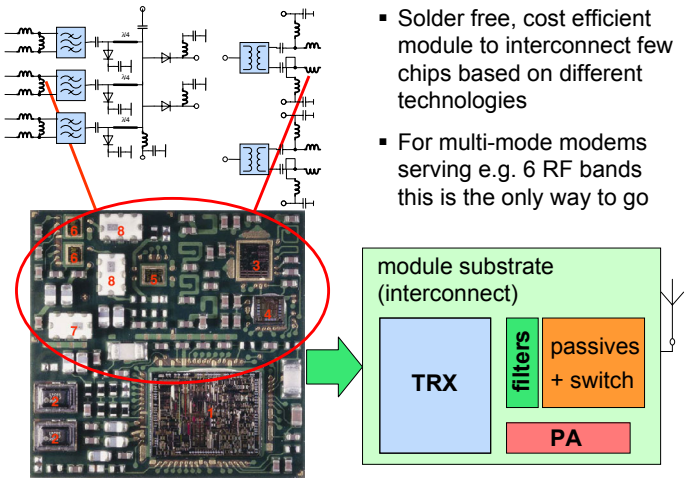

Figure 1.2.7: Front-end architecture and module technology.

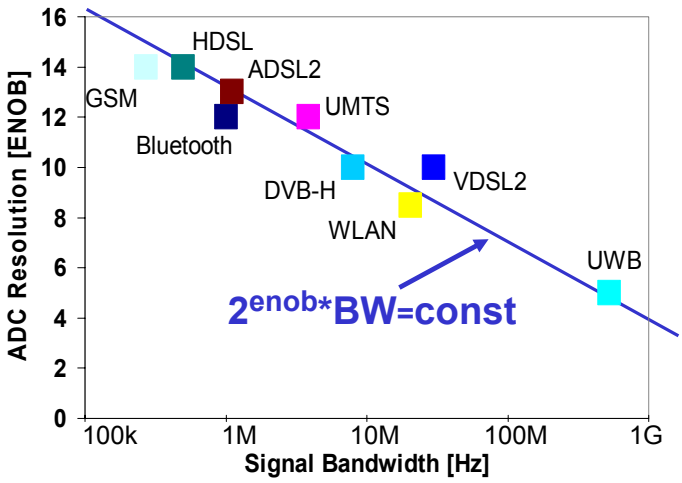

Figure 1.2.8: Signal-bandwidth and required ADC resolution.

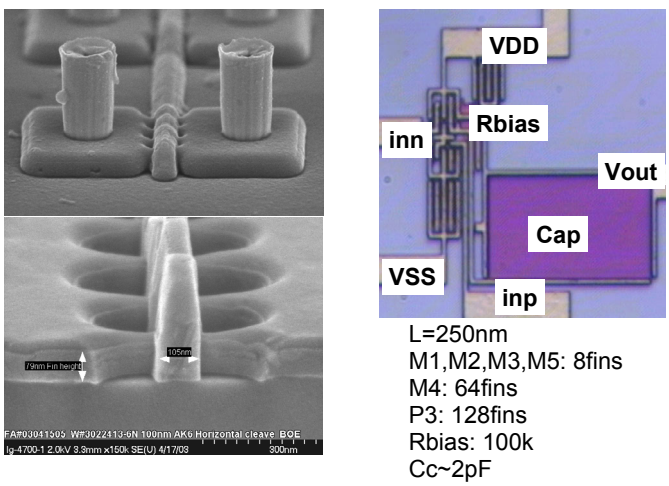

Figure 1.2.9: Operational amplifier with FinFET's

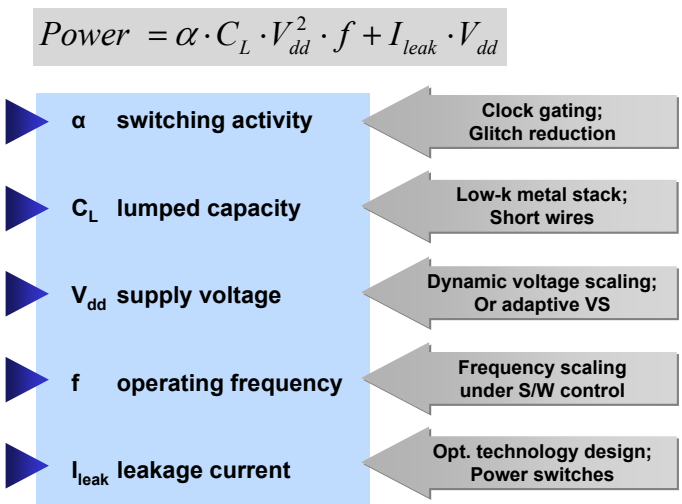

Figure 1.2.10: Low-power digital-design parameters.

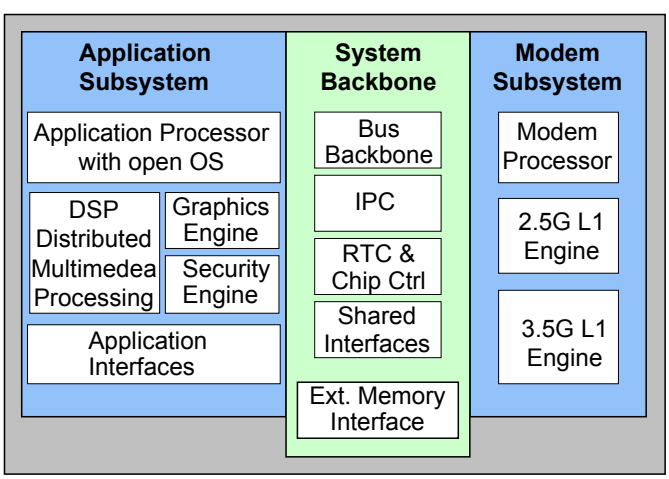

Figure 1.2.11: Baseband processor architecture at a glance.

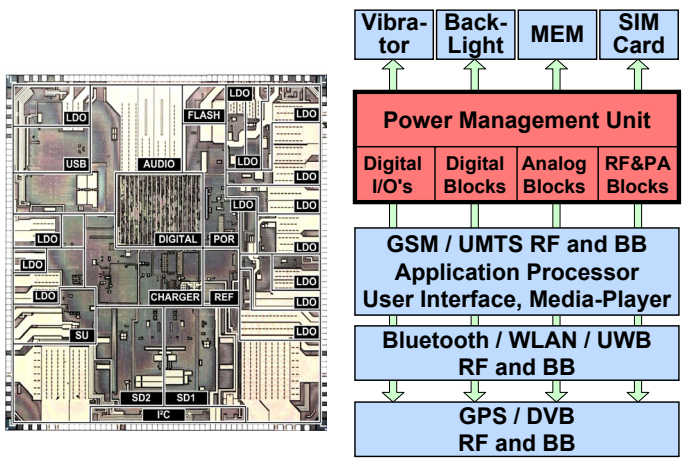

Figure 1.2.12: Power management unit for mobile phones.